Multiple Choice Questions

Chapter 4: MOS and CMOS Logic

1. How many MOSFETs are present in the circuit?
   a) 1
   b) 2
   c) 3
   d) 4

2. What is the logic level of A when the circuit is at equilibrium?
   a) 0
   b) 1
   c) Indeterminate
   d) Cannot be determined

3. Convert the decimal number 1275 into its binary equivalent.
   a) 10011000111
   b) 10010100000
   c) 10100110001
   d) 11001011100

4. Which of the following is a valid logic gate symbol for an AND gate?
   a) ![AND gate symbol]
   b) ![OR gate symbol]
   c) ![NAND gate symbol]
   d) ![NOT gate symbol]

Chapter 5: Logic Families

1. Which logic family is used in most microprocessors today?
   a) NAND
   b) CMOS
   c) TTL
   d) ECL

2. What is the advantage of CMOS logic over other families?
   a) High speed
   b) Low power consumption
   c) High noise immunity
   d) Low cost

Chapter 6: Sequential Circuits

1. What is the primary difference between a flip-flop and a latch?
   a) Storage capability
   b) Speed of operation
   c) Number of inputs
   d) Number of outputs

2. Which of the following is an example of a synchronous sequential circuit?
   a) Shift register
   b) Finite state machine
   c) Memory
   d) Multiplexer

Chapter 7: Number Systems

1. Convert the hexadecimal number 1F to its binary equivalent.
   a) 1111
   b) 1011
   c) 0111
   d) 0101

2. Which of the following statements is true about binary numbers?
   a) They are always less than 10.
   b) They cannot be negative.
   c) They can be negative.
   d) They are always positive.

Chapter 8: Digital Electronics

1. What is the purpose of a decoder?
   a) To convert a binary number into its decimal equivalent.
   b) To convert a decimal number into its binary equivalent.
   c) To convert a binary number into its hexadecimal equivalent.
   d) To convert a decimal number into its hexadecimal equivalent.

2. What is the function of a counter?
   a) To count objects
   b) To convert binary to decimal
   c) To convert decimal to binary
   d) To convert hexadecimal to binary

Chapter 9: Logic Design

1. Which logic gate is used to implement the function F = A'B + AB'
   a) ![XOR gate]
   b) ![XNOR gate]
   c) ![OR gate]
   d) ![AND gate]
TC. Consider the addition of numbers with different bases.

\[ x = \text{base } A \times (a_1a_2a_3 ... a_n) \]

Find the value of 'x.'

**Try Yourself:**

**Question:**

- 10. The decimal equivalent of octal number [7]
- 11. The decimal equivalent of hexadecimal number [E666]
- 12. The decimal equivalent of binary number [100001]
- 13. The decimal equivalent of ternary number [0101101110]
### Multiple Choice Questions

**Q.1:** Consider the Boolean expression:

\[
I = Z \land (D) \quad \text{O} = Z \lor (D) \\
Z = \lambda (A) \quad Z = \lambda (A) \\
\text{where} \quad I = \lambda (A) \lor (B) \quad \text{and} \quad (A) \lor (B) \quad \text{are} \quad \text{given}\]

Which of the following is the correct expression for \( I + O \)?

- (a) \( I + O = \lambda (A) \lor (B) \)
- (b) \( I + O = Z \lor (D) \)
- (c) \( I + O = Z \land (D) \)
- (d) \( I + O = \lambda (A) \lor (B) \)

---

### Problem 10

**Problem 10:**

The Boolean expression for the circuit in the figure is:

- (a) \( Y = \bar{X} \land (Z') \land (X') \)
- (b) \( Y = X \land (Z') \land (X') \)
- (c) \( Y = X \lor (Z') \land (X') \)
- (d) \( Y = \bar{X} \lor (Z') \land (X') \)

---

### Problem 11

**Problem 11:**

The output of the circuit in the figure is:

- (a) \( Z = X \lor (Y') \land (Y') \)
- (b) \( Z = X \land (Y') \land (Y') \)
- (c) \( Z = X \land (Y') \lor (Y') \)
- (d) \( Z = \bar{X} \land (Y') \lor (Y') \)

---

### Problem 12

**Problem 12:**

The truth table for the circuit in the figure is:

<table>
<thead>
<tr>
<th>( X )</th>
<th>( Y )</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)

---

### Problem 13

**Problem 13:**

The circuit in the figure is a combination of the following:

- (a) \( X \land (Y') \land (Y') \)
- (b) \( X \lor (Y') \land (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \lor (Y') \)

---

### Problem 14

**Problem 14:**

The circuit in the figure is a combination of the following:

- (a) \( 0 \lor (X') \land (X') \)
- (b) \( 1 \lor (X') \land (X') \)
- (c) \( 0 \lor (X') \lor (X') \)
- (d) \( 1 \lor (X') \lor (X') \)

---

### Problem 15

**Problem 15:**

The circuit in the figure is a combination of the following:

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)

---

### Problem 16

**Problem 16:**

The circuit in the figure is a combination of the following:

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)

---

### Problem 17

**Problem 17:**

The circuit in the figure is a combination of the following:

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)

---

### Problem 18

**Problem 18:**

The circuit in the figure is a combination of the following:

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)

---

### Problem 19

**Problem 19:**

The circuit in the figure is a combination of the following:

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)

---

### Problem 20

**Problem 20:**

The circuit in the figure is a combination of the following:

- (a) \( X \lor (Y') \land (Y') \)
- (b) \( X \land (Y') \lor (Y') \)
- (c) \( X \lor (Y') \lor (Y') \)
- (d) \( X \land (Y') \land (Y') \)
O.25 It is incorrect to put the circuit in the figure if \( C = 0 \) the gate \( G \) and in the figure where \( G = 0 \), the gate is not.

**Fault-2002**

\[ H + d = (a) \quad H + d = (b) \quad H + d = (c) \]

**Fault-2003**

\[ \text{The logical circuit of figure is a} \quad A = X + Y \quad A = X + Y \quad A = X + Y \]

The following is the correct letter for the figure:

\[ A = X + Y \]

**Fault-1999**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2014**

\[ (a) \quad (b) \quad (c) \quad (d) \quad (e) \quad (f) \quad (g) \quad (h) \quad (i) \quad (j) \]

\[ A B + C D = (a) \quad A B + C D = (b) \quad A B + C D = (c) \quad A B + C D = (d) \quad A B + C D = (e) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

The function is: \[ A B \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2009**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

\[ A B \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]

**Fault-2000**

\[ (p) \quad (q) \quad (r) \quad (s) \quad (t) \quad (u) \quad (v) \quad (w) \quad (x) \quad (y) \]
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20.1 Introduction to Digital Logic Design

20.2 Logic Gates and Boolean Algebra

20.3 Logic Families

20.4 Logic Minimization

20.5 Combinational Logic Design

20.6 Sequential Logic Design

20.7 Interfacing with the Microprocessor

20.8 Digital System Design

20.9 Digital System Verification and Testing

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21.4 Interrupts and DMA

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21.6 Embedded System Design

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26.4 Software Engineering

26.5 Testing and Debugging
Combinational Logic Circuits
Consider the two sorted 2-to-1 multiplexers.

\[ \text{(a)} \quad y_{1} = \left( \overline{z} \cdot \overline{A} \right) \lor \left( z \cdot A \right) \]

\[ \text{(b)} \quad y_{2} = \left( \overline{z} \cdot \overline{B} \right) \lor \left( z \cdot B \right) \]

\[ \text{(c)} \quad y_{3} = \left( \overline{z} \cdot \overline{C} \right) \lor \left( z \cdot C \right) \]

\[ \text{(d)} \quad y_{4} = \left( \overline{z} \cdot \overline{D} \right) \lor \left( z \cdot D \right) \]

\[ \text{(e)} \quad y_{5} = \left( \overline{z} \cdot \overline{E} \right) \lor \left( z \cdot E \right) \]

\[ \text{(f)} \quad y_{6} = \left( \overline{z} \cdot \overline{F} \right) \lor \left( z \cdot F \right) \]

\[ \text{(g)} \quad y_{7} = \left( \overline{z} \cdot \overline{G} \right) \lor \left( z \cdot G \right) \]

\[ \text{(h)} \quad y_{8} = \left( \overline{z} \cdot \overline{H} \right) \lor \left( z \cdot H \right) \]

\[ \text{(i)} \quad y_{9} = \left( \overline{z} \cdot \overline{I} \right) \lor \left( z \cdot I \right) \]

\[ \text{(j)} \quad y_{10} = \left( \overline{z} \cdot \overline{J} \right) \lor \left( z \cdot J \right) \]

The output of the multiplexer is given by

\[ y = \left( \overline{z} \cdot y_{i} \right) \lor \left( z \cdot y_{i} \right) \quad \text{for} \quad i = 1, 2, \ldots, 10 \]
The digital output inverter function will be performed by inverting the corresponding digital output signal. The inverter function can be expressed as:

\[ \text{Output} = \neg \text{Input} \]

where \( \neg \) represents the logical NOT operation.

The number of 2-input NAND gates required to implement the inverter function is:

\[ \text{Number of gates} = n \times 2 \]

where \( n \) is the number of inputs to the inverter.

The decoder is used to select one of the \( 2^n \) inputs. The number of decoder inputs required is:

\[ \text{Number of decoder inputs} = \log_2 n \]

The decoder is expressed as:

\[ \text{Decoder outputs} = \{0, 1, \ldots, \log_2 n\} \]

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The decoder is expressed as:

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\[ \text{Number of decoder inputs} = \log_2 n \]

The decoder is expressed as:

\[ \text{Decoder outputs} = \{0, 1, \ldots, \log_2 n\} \]
Sequential Circuits

Multiple Choice Questions

10. The characteristic equation of the flip-flop is given by:
   \[ Q^+ = Q \cdot \overline{D} + Q \cdot D \]

11. Consider the circuit below. The input X should be:
   \[ X = \overline{Z} \cdot \overline{A} + \overline{Z} \cdot A \]

12. For the given multiplexer, the output Y is equal to:
   \[ Y = \overline{B} \cdot C + B \cdot C \]

13. The equation for the circuit is:
   \[ Y = \overline{B} \cdot C + B \cdot C \]

14. The minimised expression for \( Y \) is:
   \[ Y = \overline{B} \cdot C + B \cdot C \]

15. The circuit diagram below shows the connection of the multiplexer:
   \[ \text{Multiplexer Input:} \overline{B} \rightarrow 0, C \rightarrow 1 \]

16. The circuit diagram below shows the connection of the flip-flop:
   \[ \text{Flip-flop:} X \rightarrow \overline{Z}, A \rightarrow Z \]
Questions

[Image]

Numerical Fill in Type

1. [Blank]
2. [Blank]
3. [Blank]
4. [Blank]
5. [Blank]
6. [Blank]
7. [Blank]
8. [Blank]
9. [Blank]
10. [Blank]

Multiple Choice Questions

1. [Option A]
2. [Option B]
3. [Option C]
4. [Option D]
5. [Option E]
6. [Option F]
7. [Option G]
8. [Option H]
9. [Option I]
10. [Option J]

Memories

[Image]
Multiple Choice Questions

1. The equation for the or gate is:
   (a) \( A \cdot B \)
   (b) \( A + B \)
   (c) \( A \cdot B \)\( \bar{A} \cdot \bar{B} \)

2. The NAND gate is:
   (a) \( A \cdot B \)
   (b) \( A + B \)
   (c) \( \bar{A} \cdot \bar{B} \)

3. The NOR gate is:
   (a) \( A + B \)
   (b) \( A \cdot B \)
   (c) \( \bar{A} + \bar{B} \)

4. The EXCLUSIVE-OR gate is:
   (a) \( A \cdot \bar{B} + B \cdot \bar{A} \)
   (b) \( A + B \)
   (c) \( A \cdot B \)

5. The XOR gate is:
   (a) \( A \cdot \bar{B} + \bar{A} \cdot B \)
   (b) \( A \cdot B \)
   (c) \( A + B \)

6. The MOS circuit shown below is a gate of the family:
   (a) AND
   (b) OR
   (c) NOT

7. Consider the following statement: The output of a complementary MOS (CMOS) inverter is:
   (a) \( A \cdot \bar{B} + \bar{A} \cdot B \)
   (b) \( A \cdot B \)
   (c) \( A + B \)

8. Consider the following statements about the output of a CMOS inverter:
   (a) The output is always at the high level.
   (b) The output is always at the low level.
   (c) The output can be either high or low depending on the input.
Questions

1. For 4 bit DAC, the following 4 bit binary number is to be converted into equivalent decimal number. Draw the circuit diagram.

2. A 4 bit DAC operates as full scale output of 0V when the input is 1011. The output voltage is 2V when the input is 1111. Given the null point of the DAC is 0.5V, find the full scale output of the 4 bit DAC.

3. The output of the comparator is logic 1 if the voltage of the circuit is more than 0.5V. The output is logic 0 if the voltage of the circuit is less than 0.5V. Draw the circuit diagram.

4. Consider the circuit shown below.

   **The Transformer**

   ![Transformer Diagram](image)

   **Questions**

   1. The transformer primary winding has 1000 turns and the secondary winding has 200 turns. The voltage across primary is 200V. Calculate the voltage across secondary.

   2. If the primary voltage is 110V, what is the secondary voltage?

   3. Consider the circuit shown below.

   ![Circuit Diagram](image)

   **Questions**

   1. For the circuit shown, determine the output voltage.

   2. If the input voltage is 3.5V, what is the output voltage?
Architecture of INTEL 8085 Microprocessor
**Multiple Choice Questions**

**Intel 8085 and Intel 8086**

1. Which of the following is correct?
   - [ ] Option A
   - [ ] Option B
   - [ ] Option C

2. Consider the following statement: The Intel 8086 microprocessor is an improvement over the Intel 8085 microprocessor. Which of the following options correctly describes this improvement?
   - [ ] Option A
   - [ ] Option B
   - [ ] Option C

3. Which of the following statements is true regarding the Intel 8085 and Intel 8086 microprocessors?
   - [ ] Option A
   - [ ] Option B
   - [ ] Option C

4. Consider the following memory addressing technique: Which of the following options correctly describes the technique used by the Intel 8085 and Intel 8086 microprocessors?
   - [ ] Option A
   - [ ] Option B
   - [ ] Option C

5. Which of the following statements is true regarding the Intel 8085 and Intel 8086 microprocessors?
   - [ ] Option A
   - [ ] Option B
   - [ ] Option C
Microprocessors
Programming of

Multiple Choice Questions

Q1. If we have an 8086 processor, which of the following is true?
(a) It has 8-bit registers.
(b) It uses a Harvard architecture.
(c) It supports multitasking.
(d) It has a 16-bit address bus.

Q2. What is the address of the following instruction?
(a) 0000H
(b) 1000H
(c) 2000H
(d) 3000H

Q3. What is the function of the opcode?
(a) It provides the operation code.
(b) It specifies the data to be operated.
(c) It indicates the addressing mode.
(d) It determines the memory location.

Q4. Which of the following is true about the 8086 microprocessor?
(a) It supports real mode only.
(b) It supports virtual memory addresses.
(c) It has 16-bit registers.
(d) It has 8-bit ALU.

Q5. What is the use of the segment register?
(a) It provides the memory address.
(b) It stores the instruction pointer.
(c) It specifies the memory segment.
(d) It determines the memory bank.

Q6. What is the address of the following instruction?
(a) 0000H
(b) 1000H
(c) 2000H
(d) 3000H

Q7. What is the function of the opcode?
(a) It provides the operation code.
(b) It specifies the data to be operated.
(c) It indicates the addressing mode.
(d) It determines the memory location.

Q8. Which of the following is true about the 8086 microprocessor?
(a) It supports real mode only.
(b) It supports virtual memory addresses.
(c) It has 16-bit registers.
(d) It has 8-bit ALU.

Q9. What is the use of the segment register?
(a) It provides the memory address.
(b) It stores the instruction pointer.
(c) It specifies the memory segment.
(d) It determines the memory bank.

Q10. What is the address of the following instruction?
(a) 0000H
(b) 1000H
(c) 2000H
(d) 3000H

Questions

Q1. Try Questions

(a) What is the address of the following instruction?
(b) What is the function of the opcode?
(c) Which of the following is true about the 8086 microprocessor?
(d) What is the use of the segment register?

Q2. Conclusion

The 8086 microprocessor is an 16-bit microprocessor and supports real mode only. It has 16-bit registers and supports virtual memory addresses. The segment register specifies the memory segment.

Q3. Exercises

(a) Draw and explain the program counter.
(b) Explain the concept of the opcode.
(c) Draw and explain the instruction cycles.
(d) Explain the concept of the segment register.
Questions

1. Consider the following program:

```assembly
MOV A, 00H
ADD A, 01H
```

What is the value of `A` after execution?

A. 02H
B. 01H
C. 03H
D. 04H

2. Consider the following program:

```assembly
LJMP LABEL1
```

What is the next address after executing this program?

A. LABEL1
B. 0000H
C. 0002H
D. 0004H

3. Consider the following program:

```assembly
MOV A, 00H
```

What is the value of `A` after execution?

A. 00H
B. 01H
C. 02H
D. 03H

4. Consider the following program:

```assembly
MOV A, 00H
```

What is the value of `A` after execution?

A. 00H
B. 01H
C. 02H
D. 03H

5. Consider the following program:

```assembly
MOV A, 00H
```

What is the value of `A` after execution?

A. 00H
B. 01H
C. 02H
D. 03H

6. Consider the following program:

```assembly
MOV A, 00H
```

What is the value of `A` after execution?

A. 00H
B. 01H
C. 02H
D. 03H

7. Consider the following program:

```assembly
MOV A, 00H
```

What is the value of `A` after execution?

A. 00H
B. 01H
C. 02H
D. 03H

8. Consider the following program:

```assembly
MOV A, 00H
```

What is the value of `A` after execution?

A. 00H
B. 01H
C. 02H
D. 03H
Memory and I/O Interfacing
Questions

1. What is the main function of the memory chip?
2. How is the memory addressed?
3. What is the capacity of the memory?
4. What is the memory capacity of the 8085?
5. How is the memory accessed?
6. What is the memory access time?
7. How is the memory expanded?
8. What is the memory address?
9. What is the memory size?
10. What is the memory location?

Conversion Questions

1. Convert 1010 to decimal.
2. Convert 256 to binary.
3. Convert 128 to hexadecimal.
4. Convert 16 to octal.
5. Convert 30 to hexadecimal.
6. Convert 64 to octal.
7. Convert 255 to hexadecimal.
8. Convert 127 to octal.
9. Convert 8 to hexadecimal.
10. Convert 15 to octal.